

FIG. 1 (PRIOR ART)

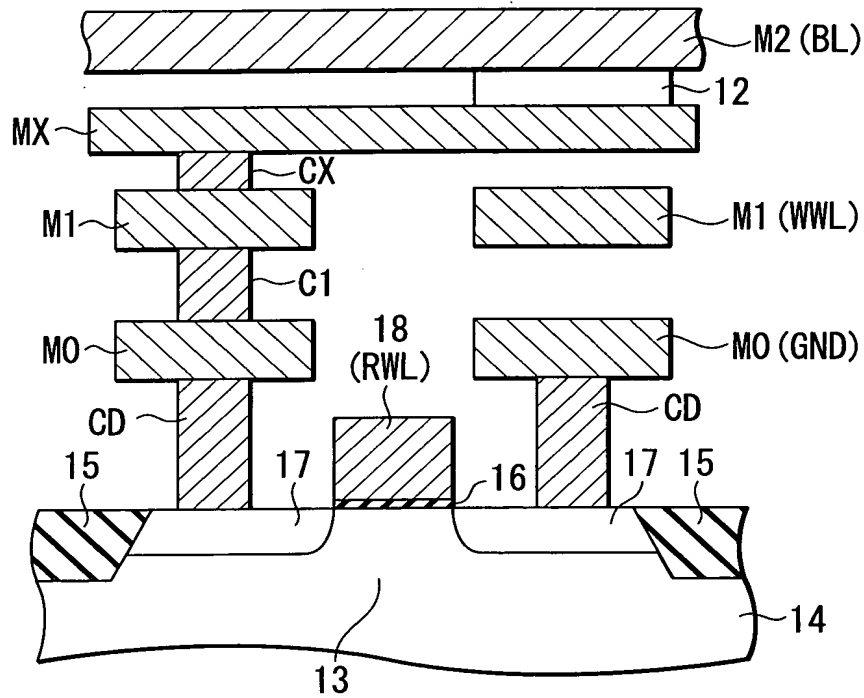


FIG. 2 (PRIOR ART)

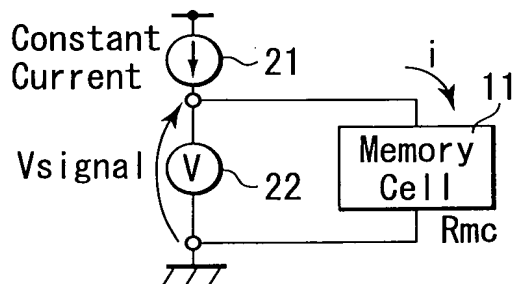


FIG. 3A (PRIOR ART)

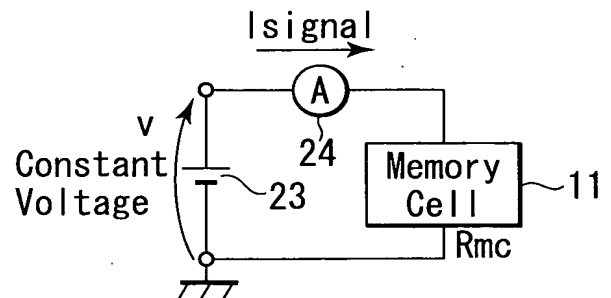


FIG. 3B (PRIOR ART)

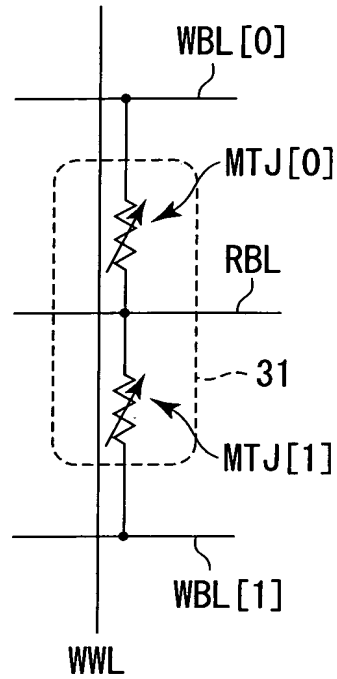


FIG. 4

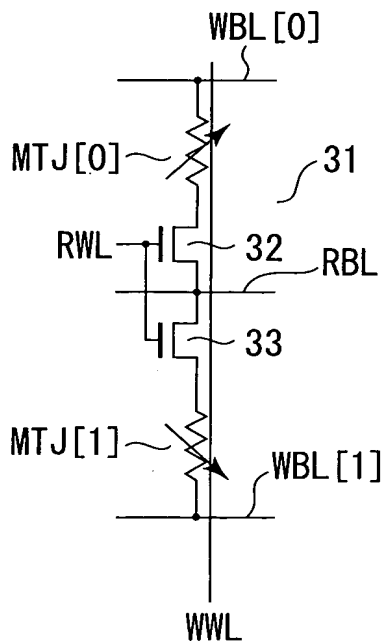


FIG. 5

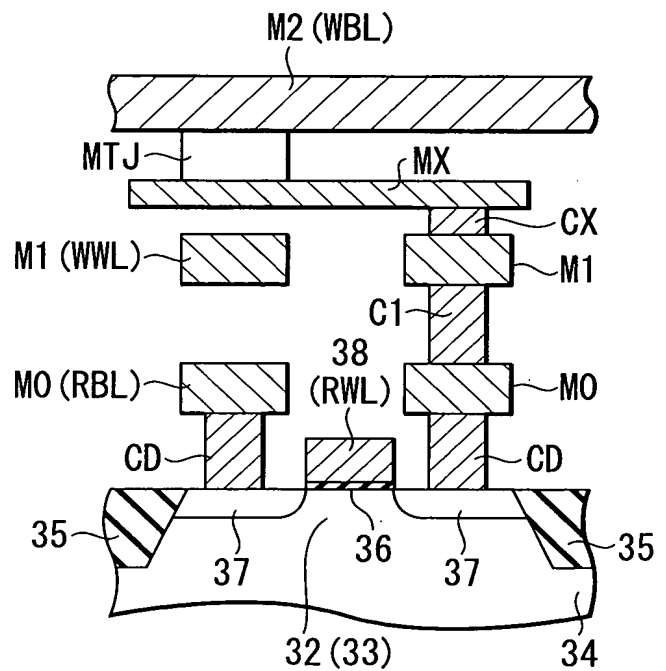


FIG. 6

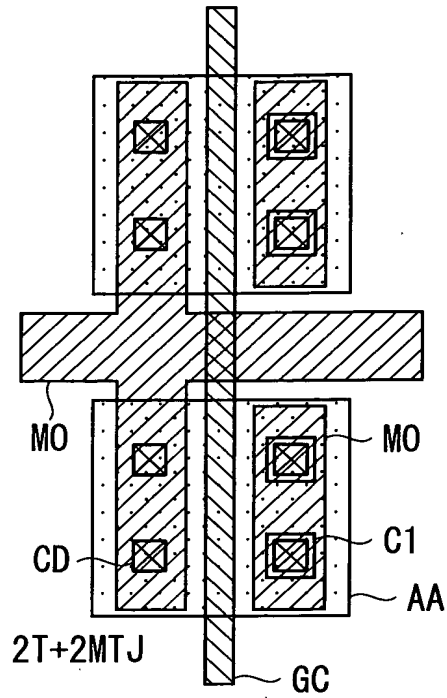


FIG. 7A

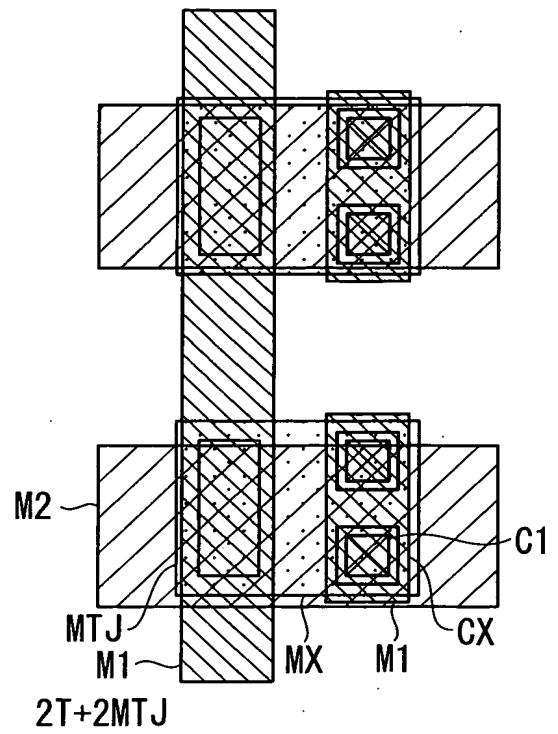


FIG. 7B

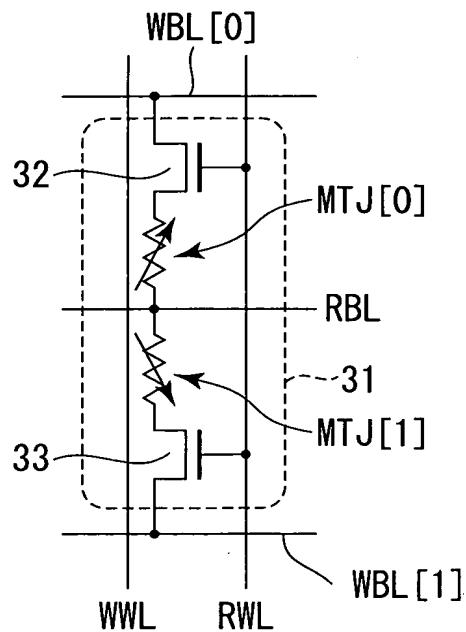


FIG. 8

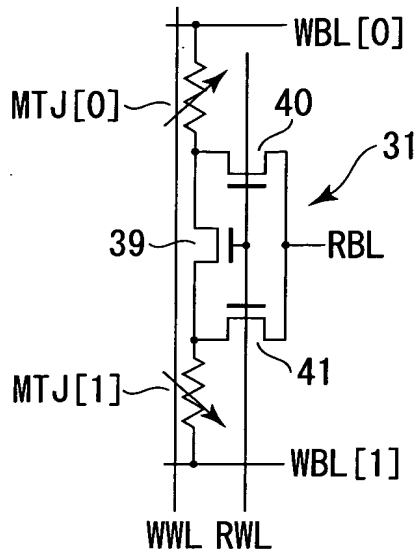


FIG. 9

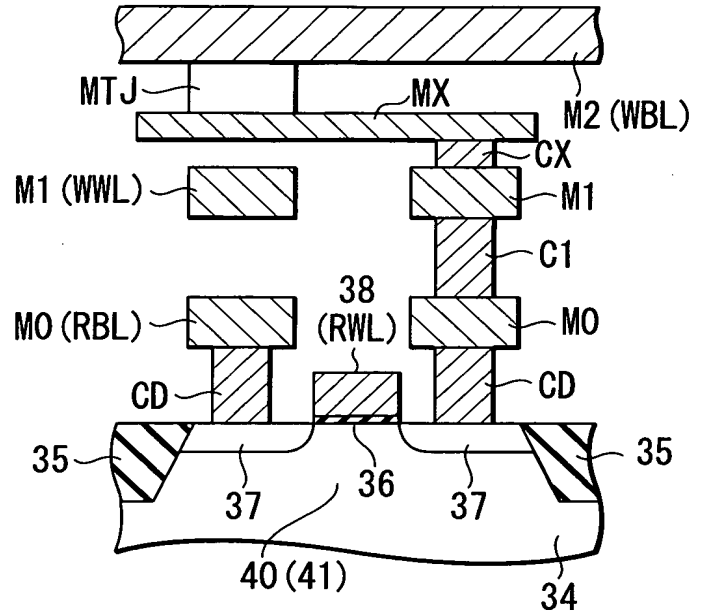


FIG. 10

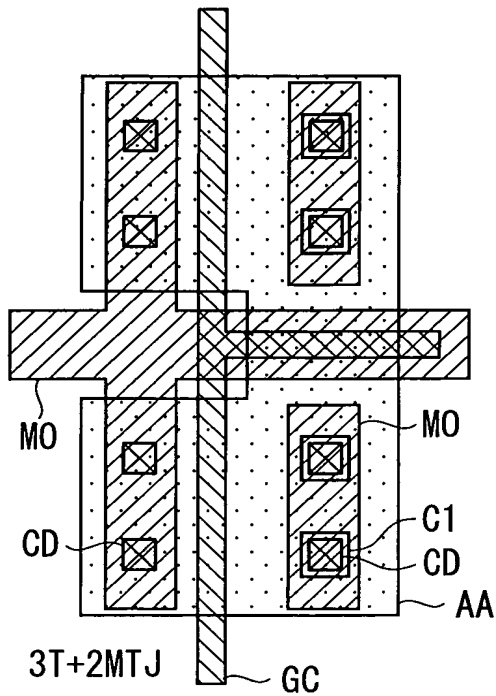


FIG. 11A

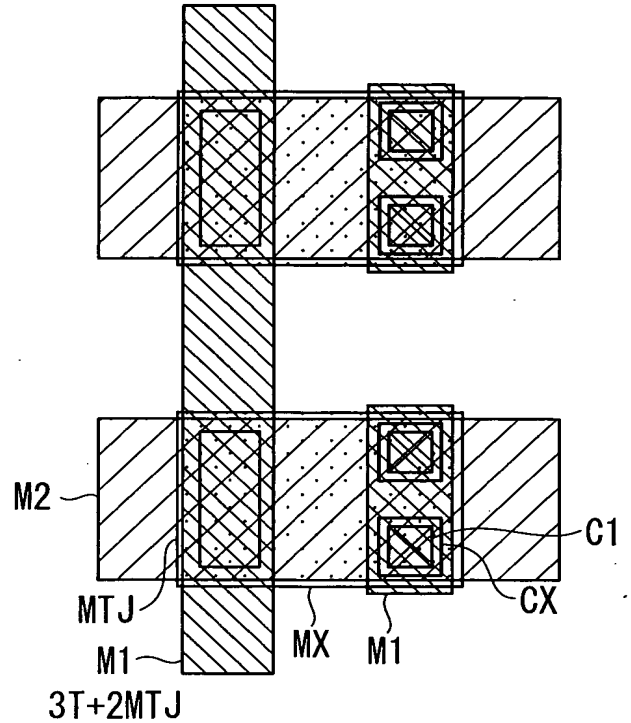


FIG. 11B

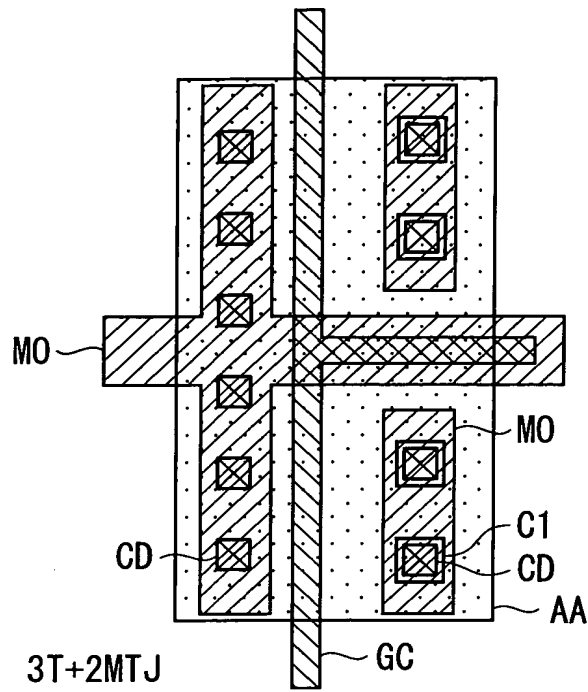


FIG. 12

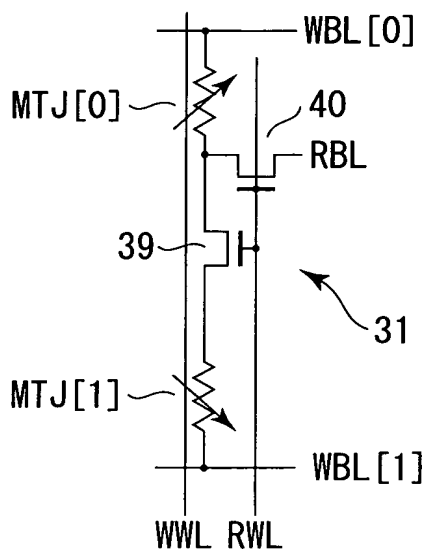


FIG. 13

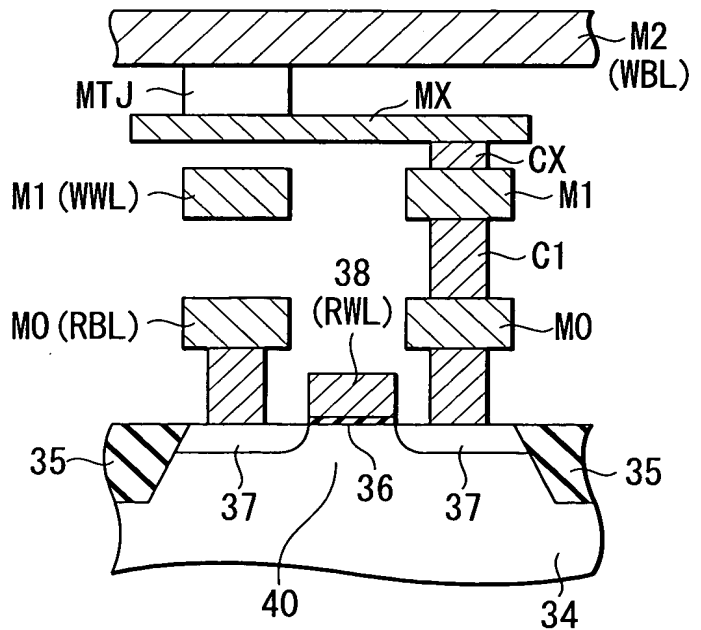


FIG. 14

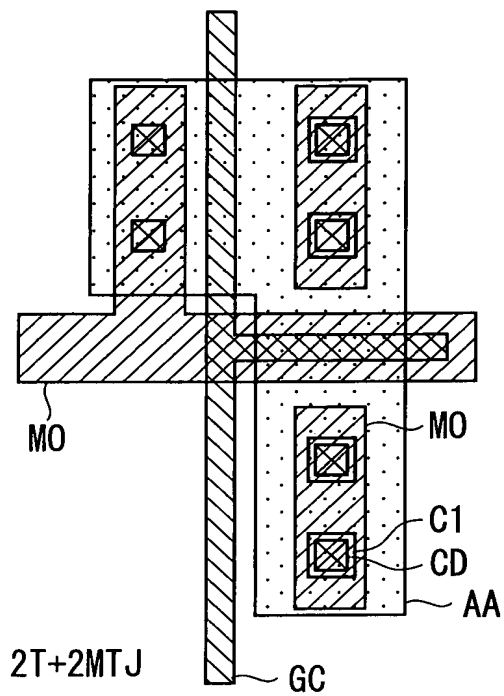


FIG. 15A

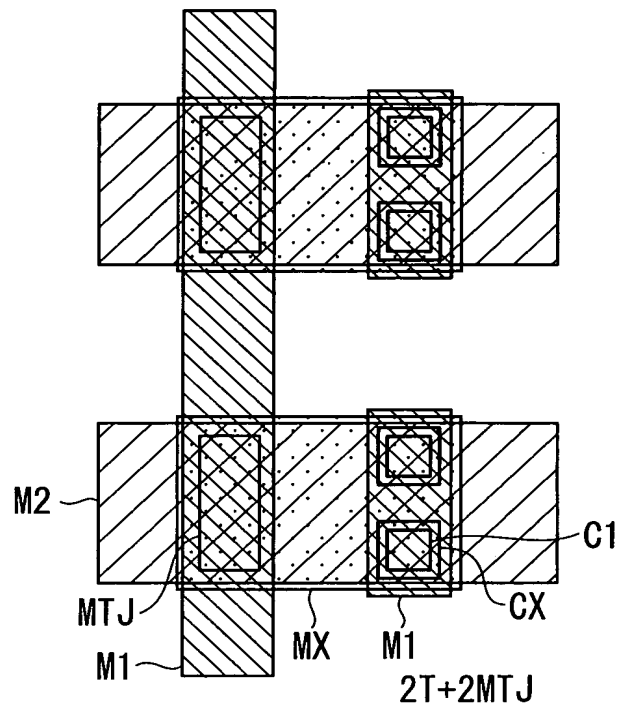


FIG. 15B

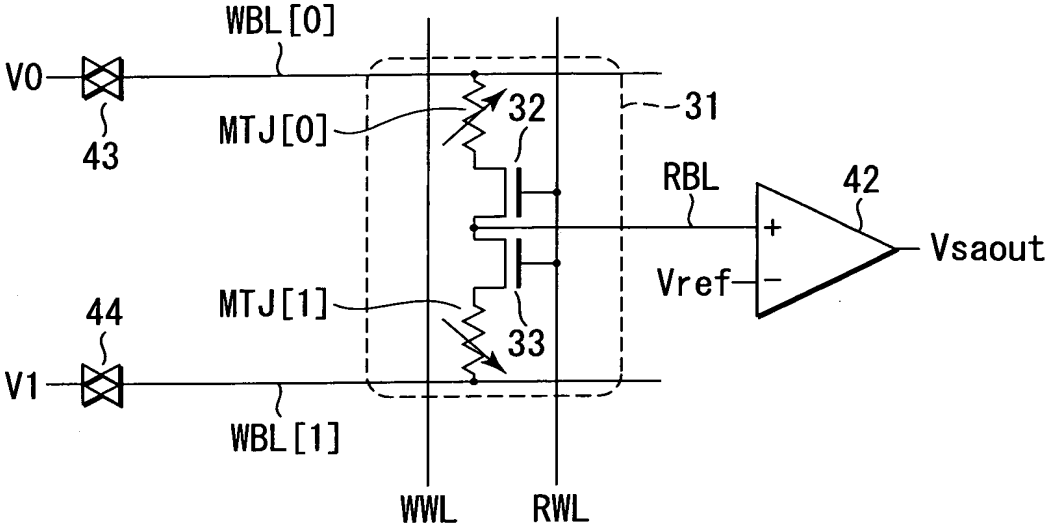


FIG. 16

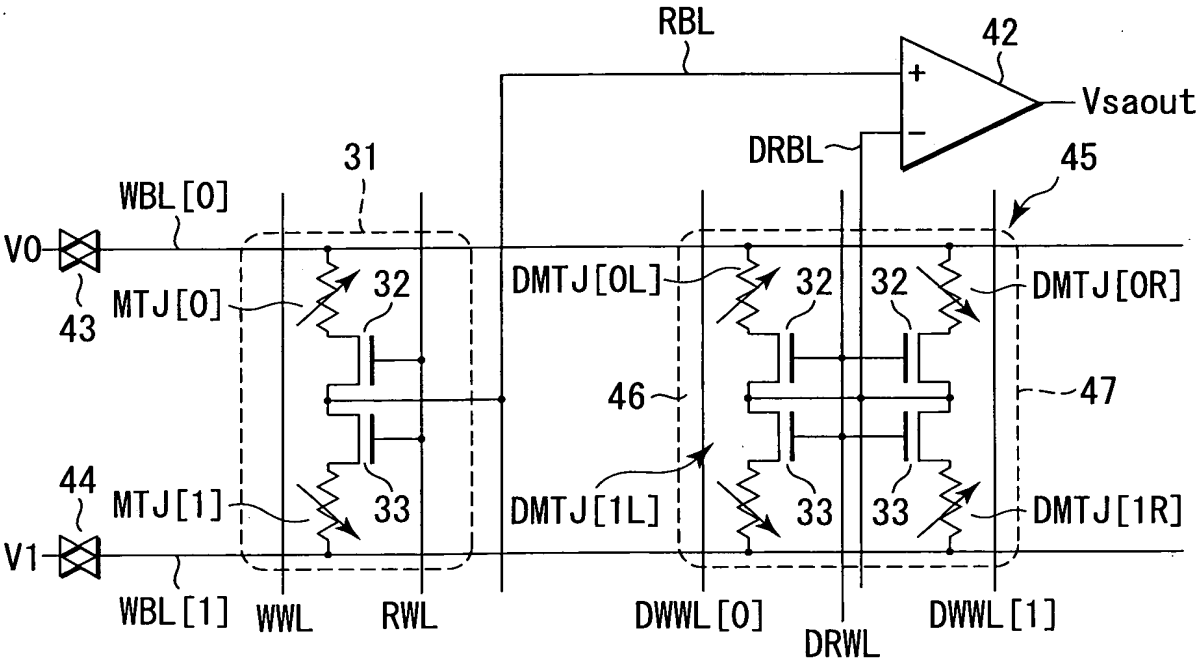


FIG. 17

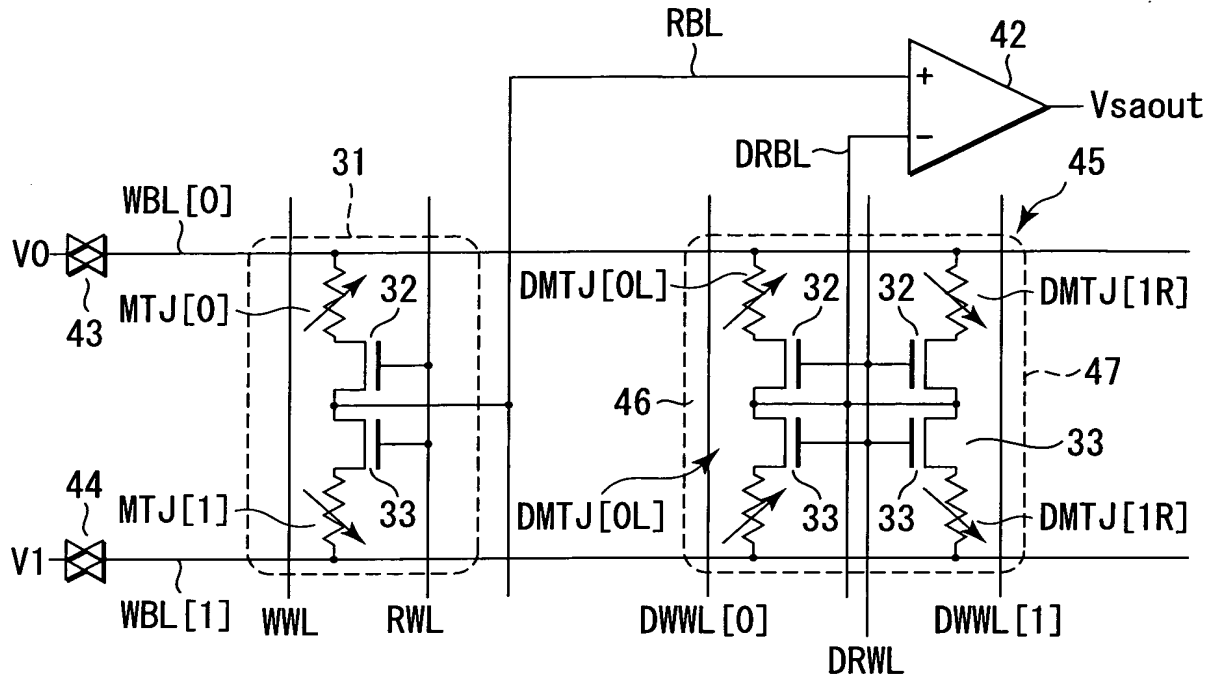


FIG. 18

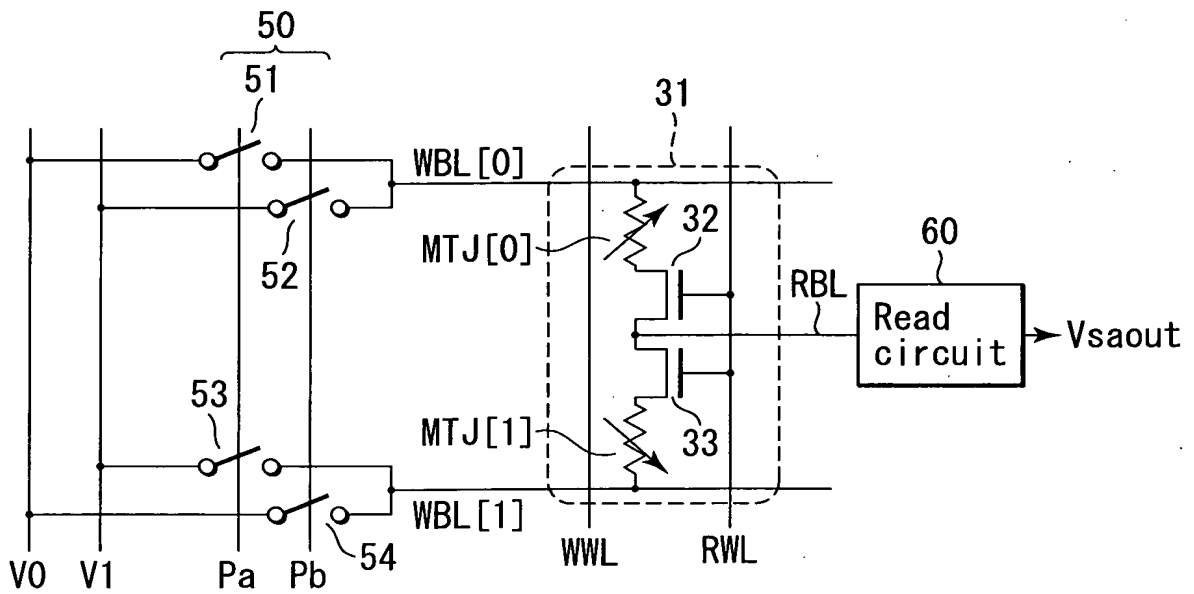


FIG. 19

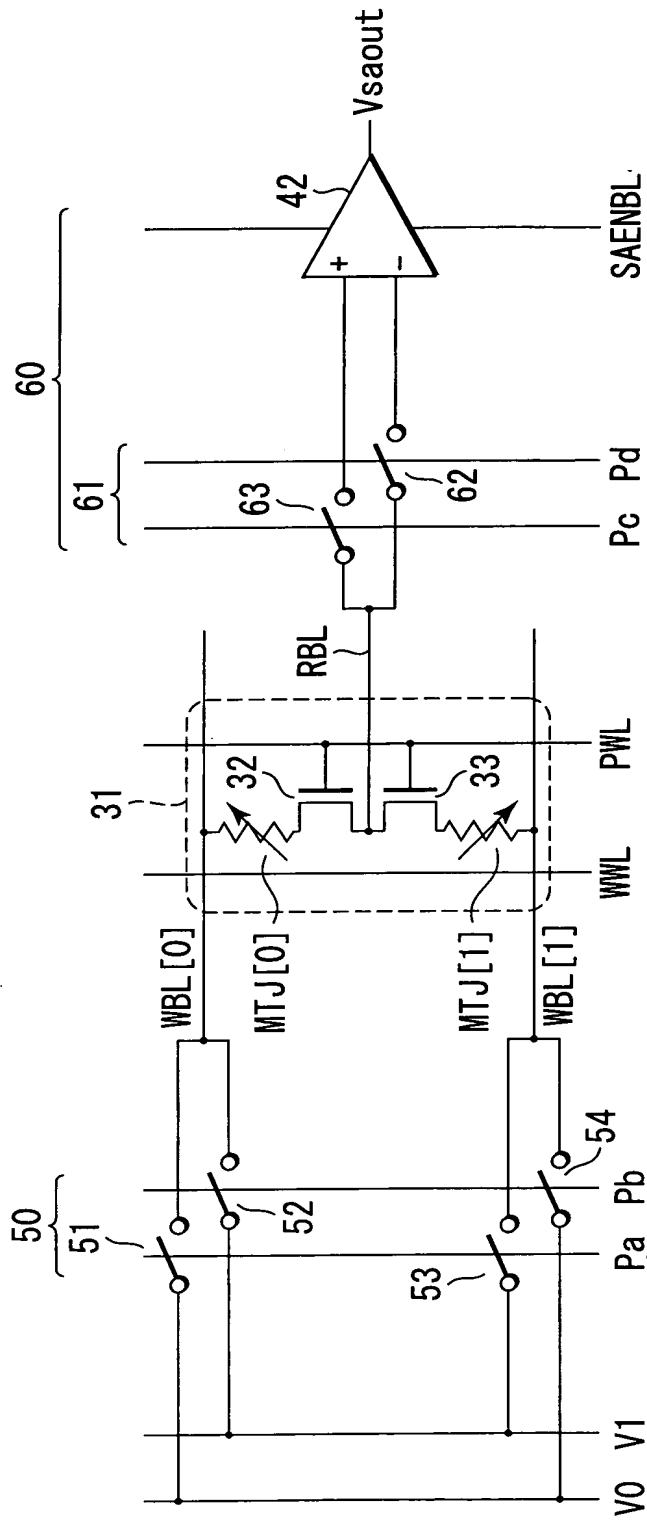


FIG. 20

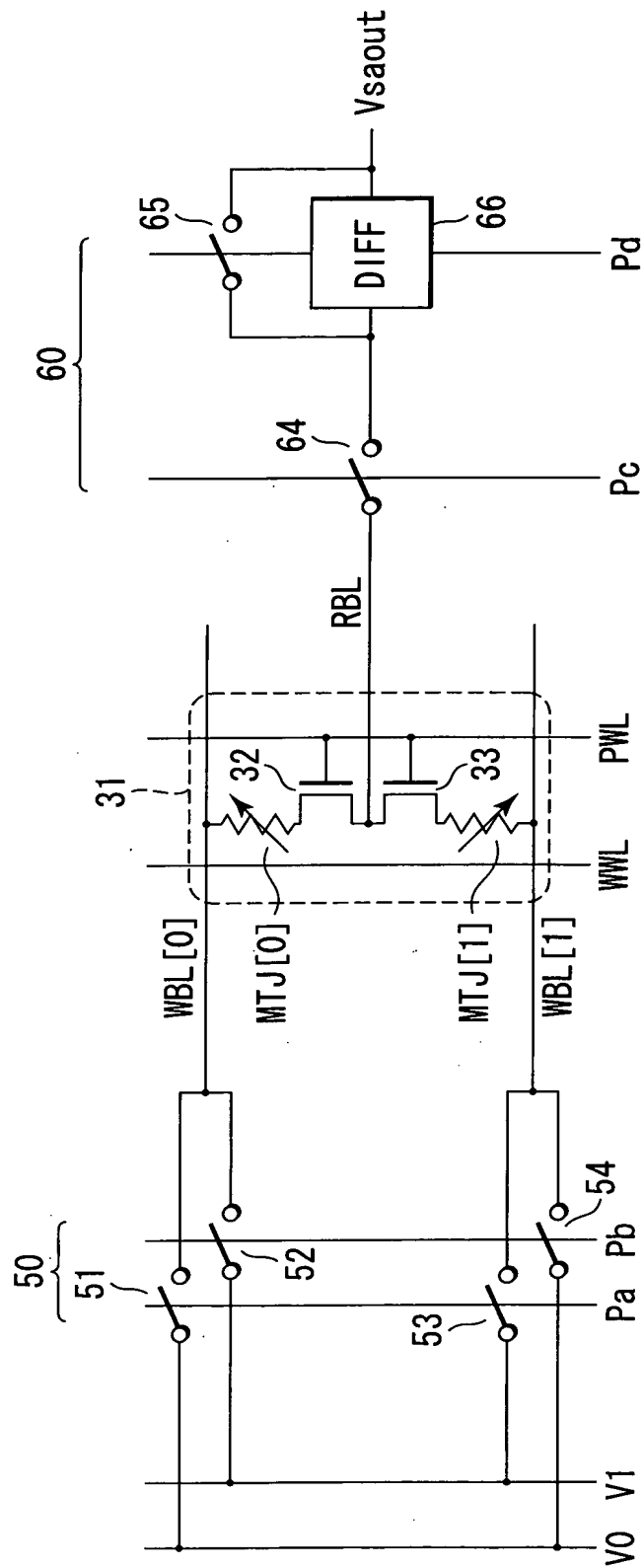
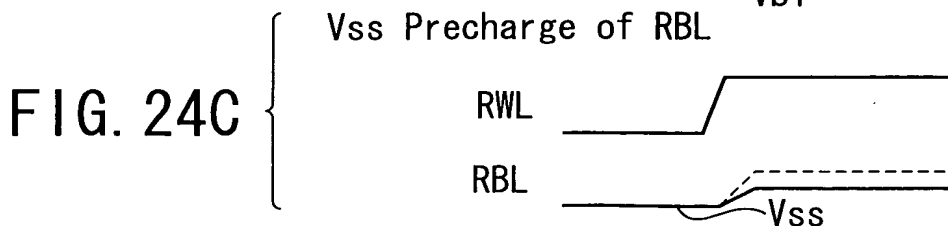
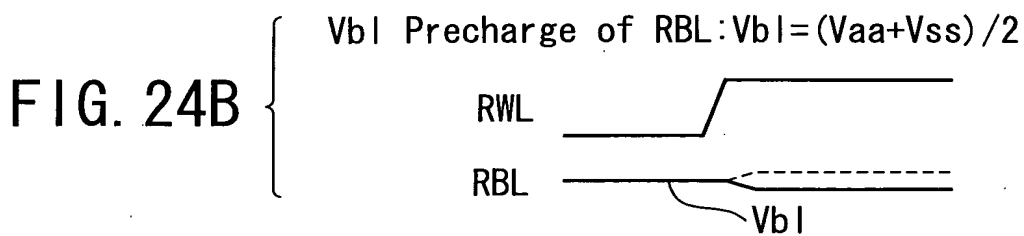
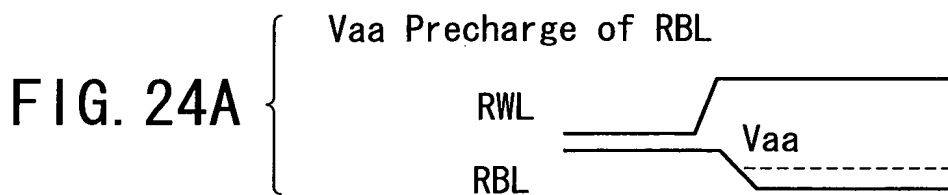
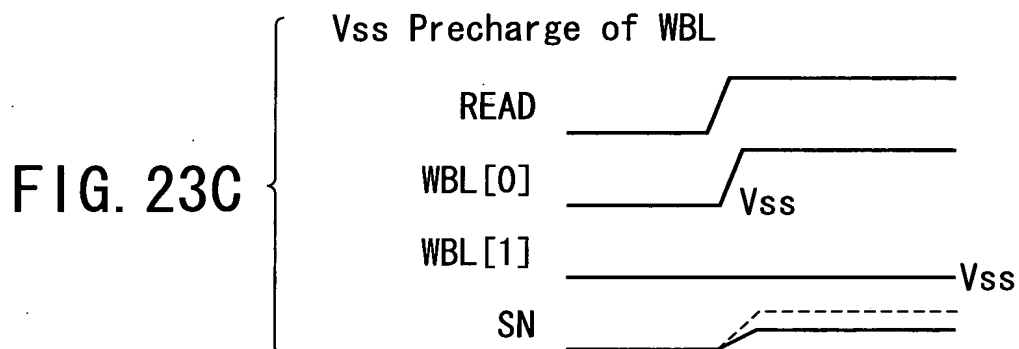
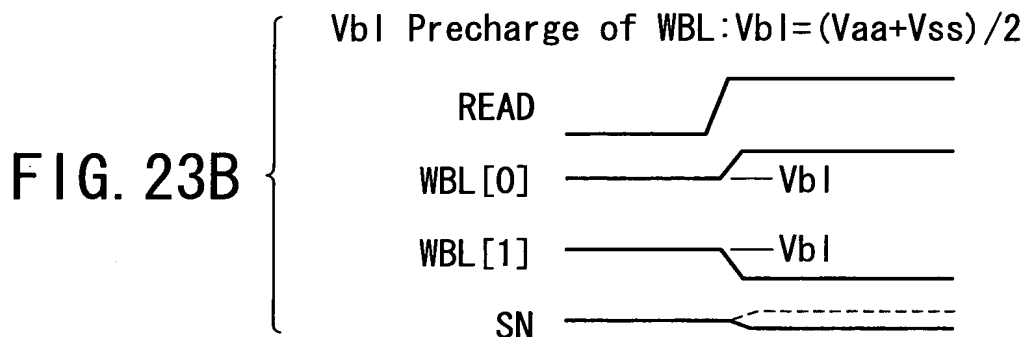
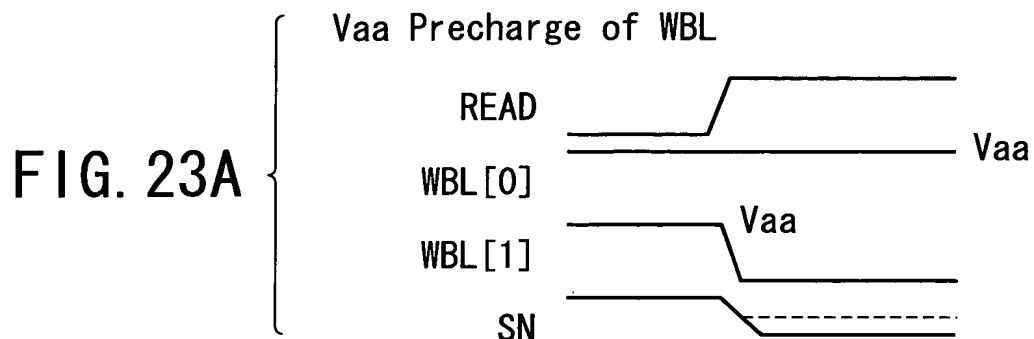


FIG. 21



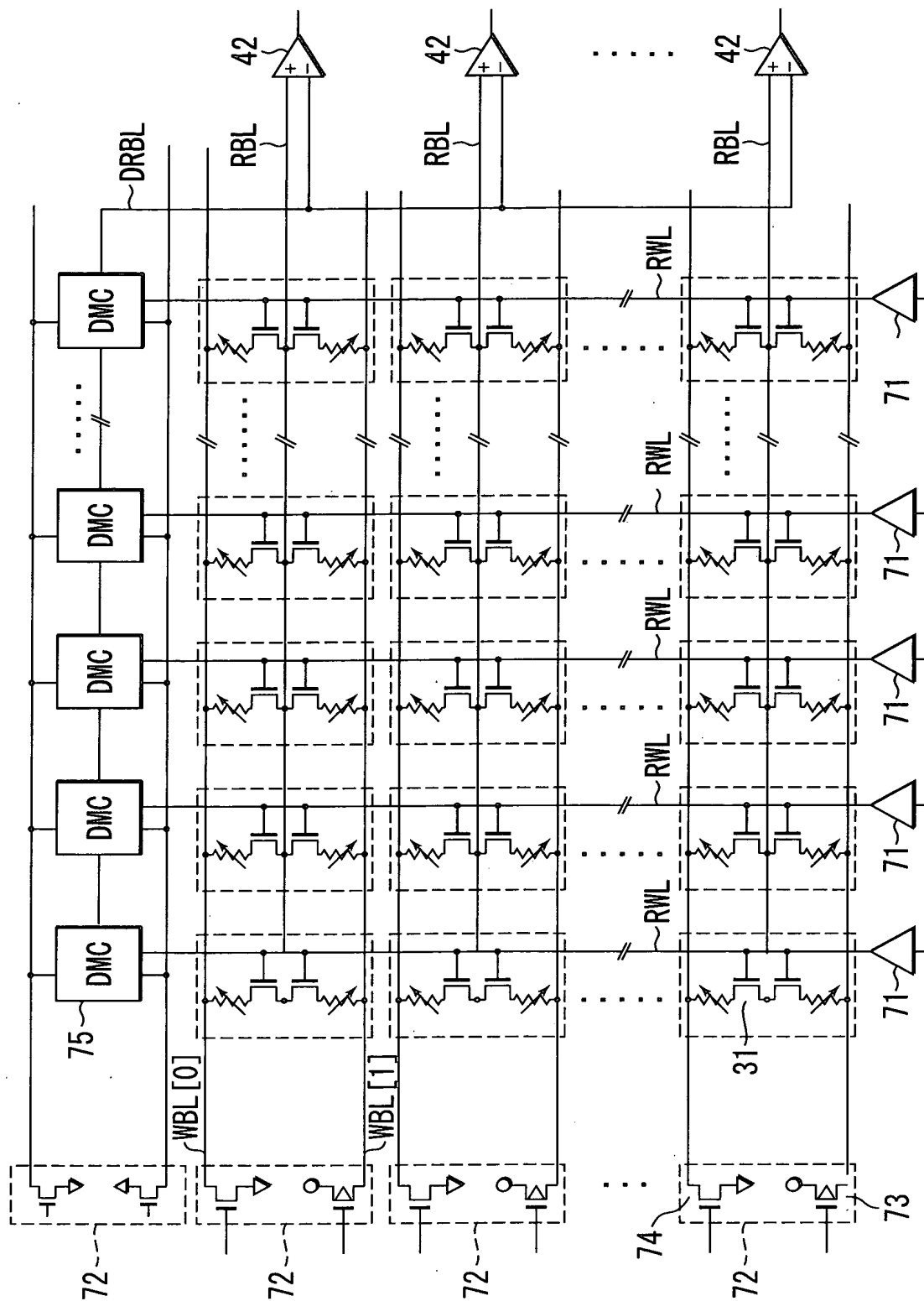


FIG. 25



FIG. 26

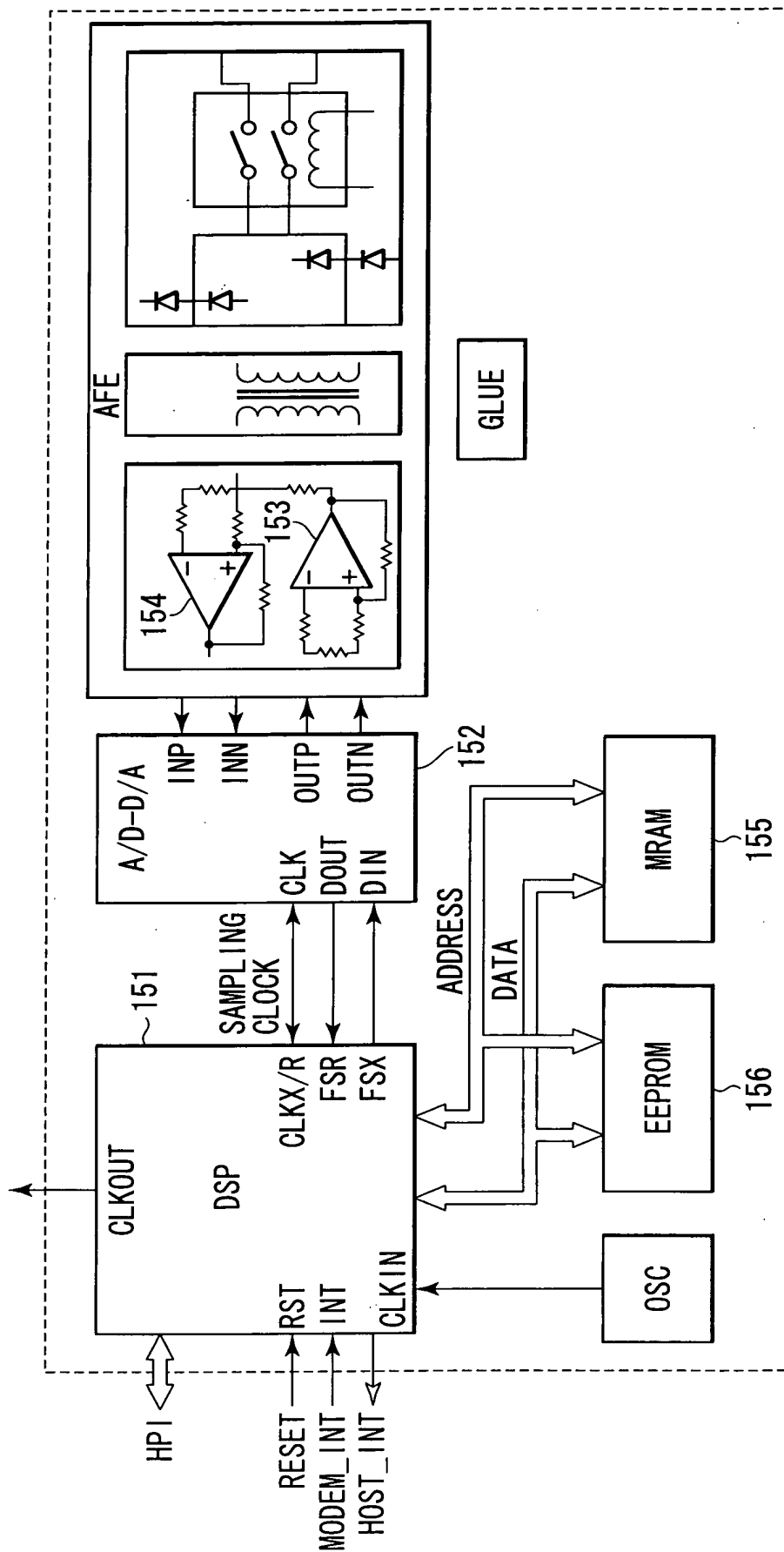


FIG. 27

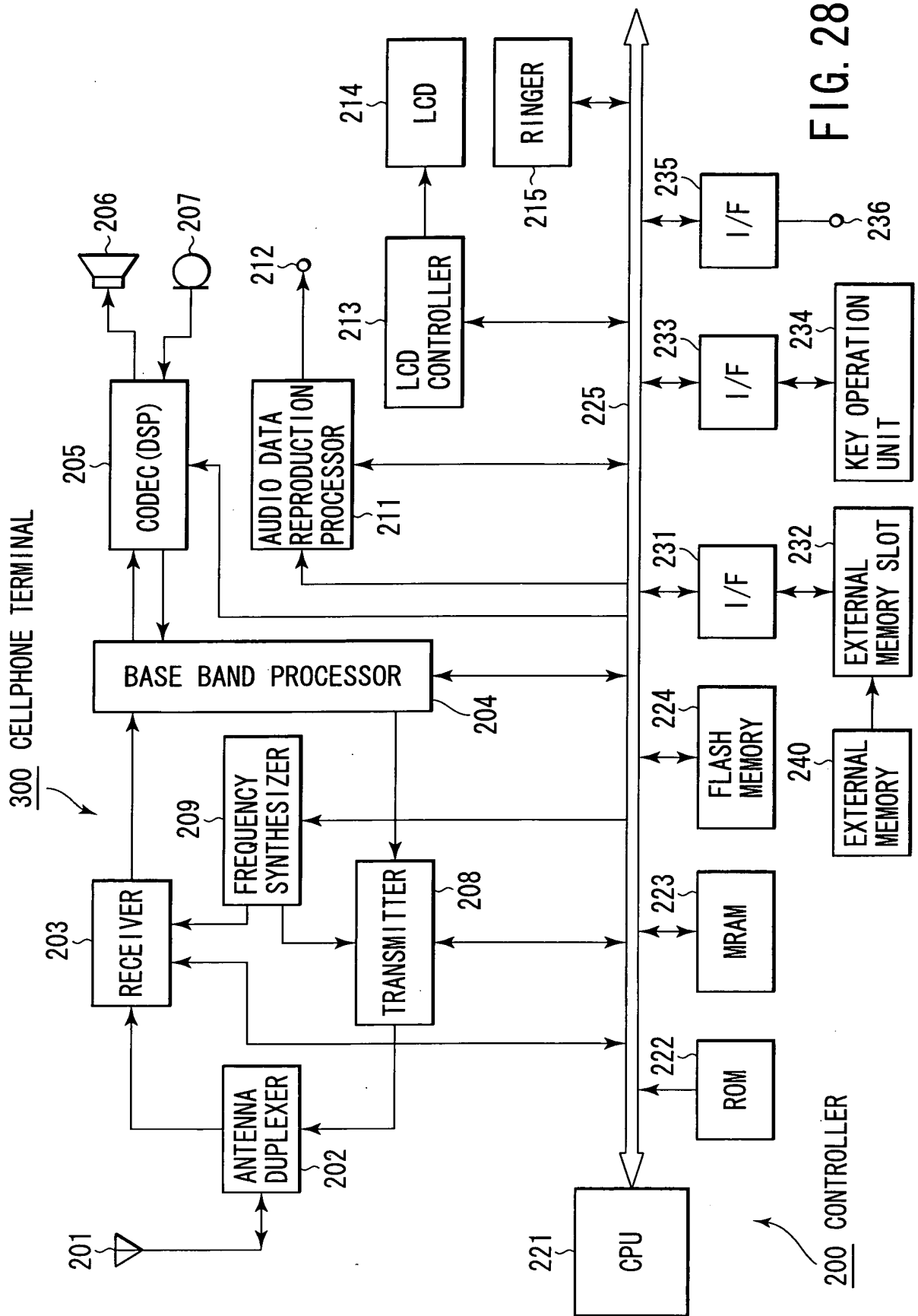


FIG. 28

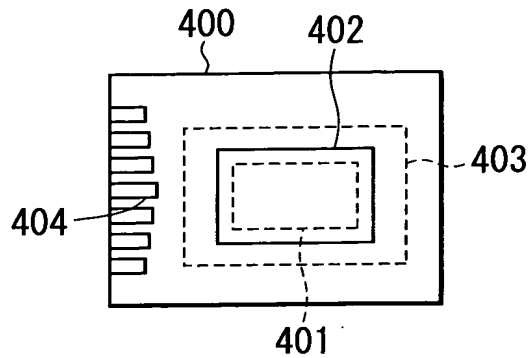


FIG. 29

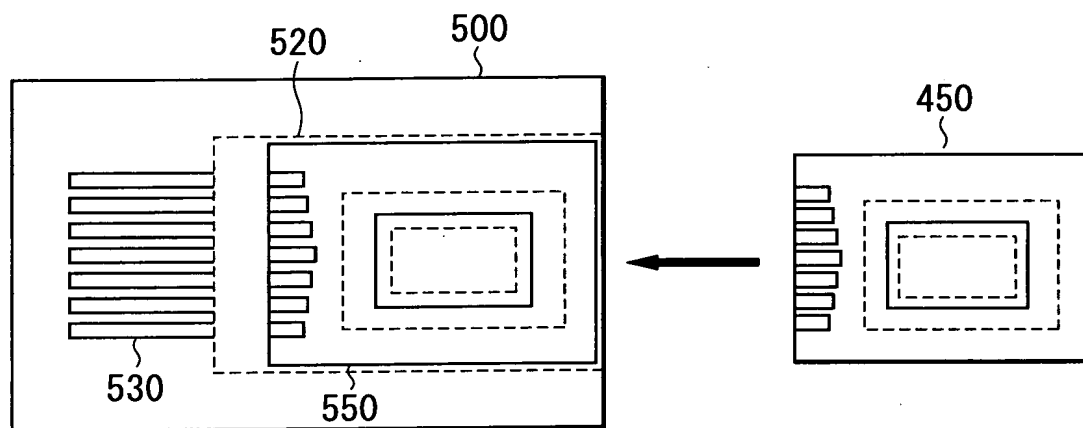
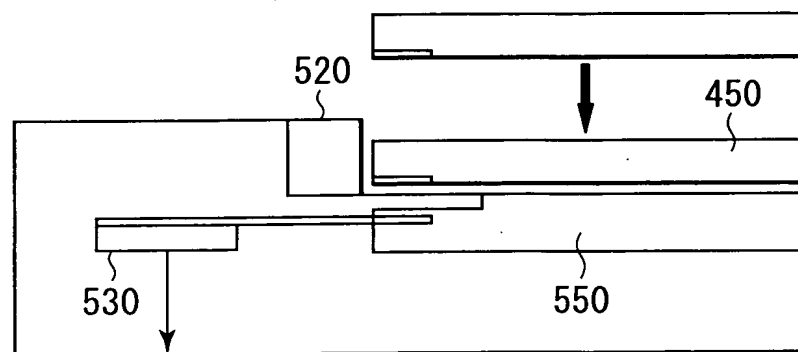


FIG. 30



TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 32

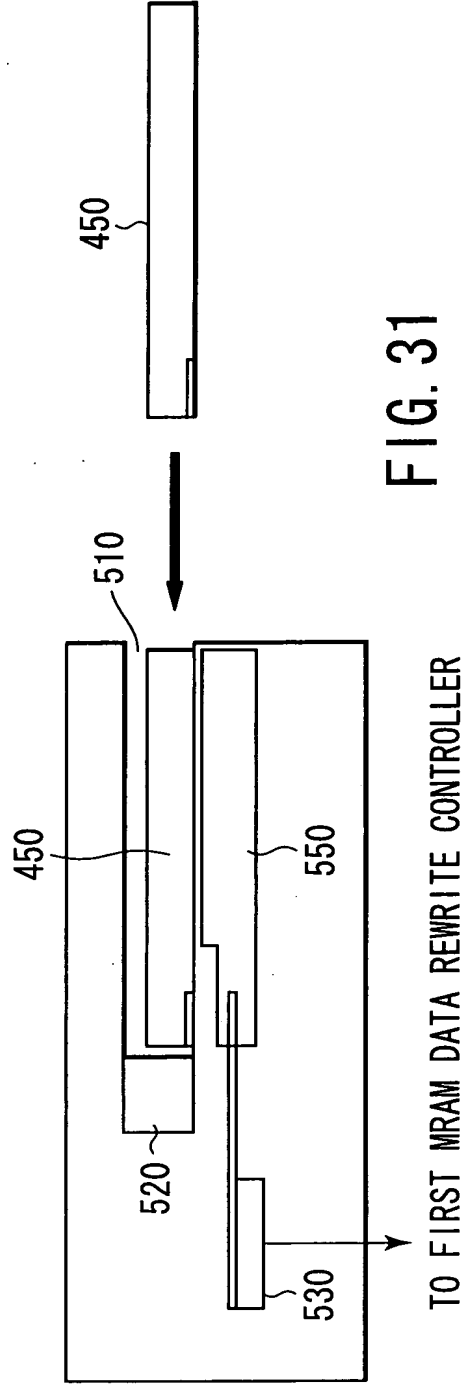


FIG. 31

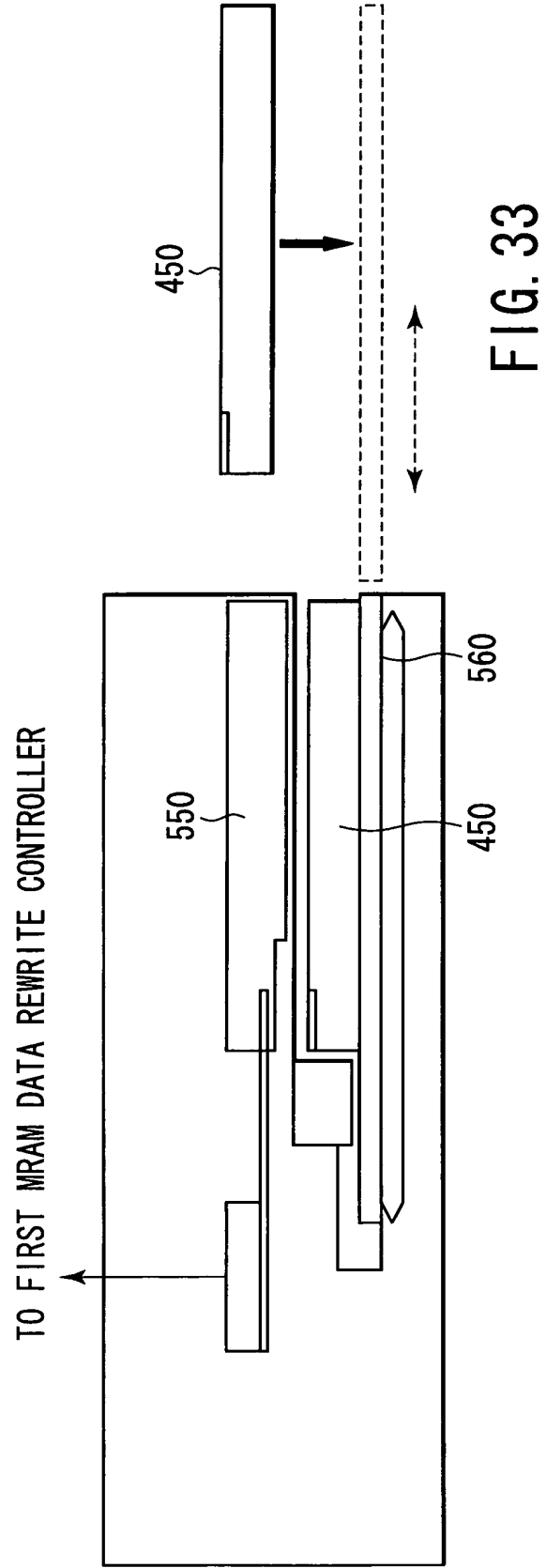


FIG. 33